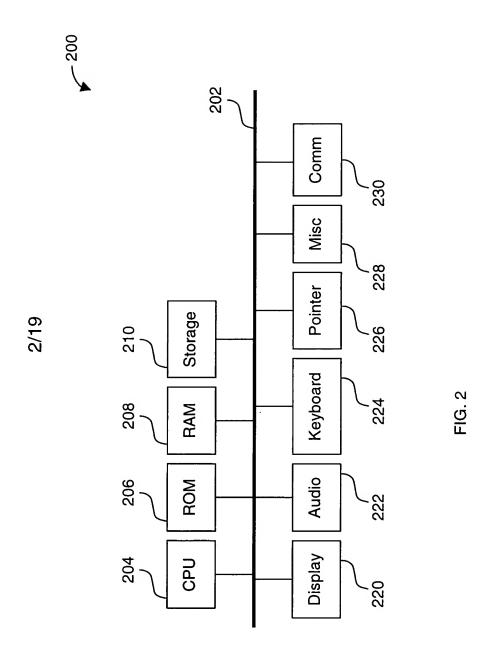
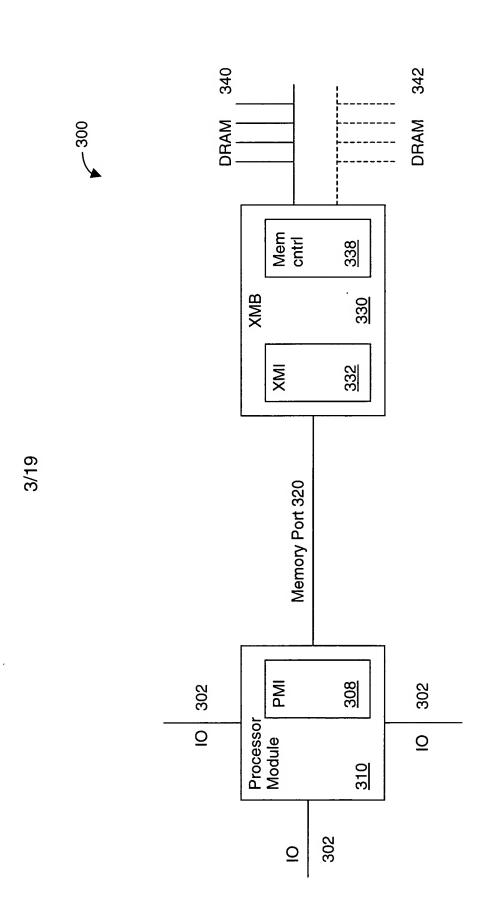


FIG. 1

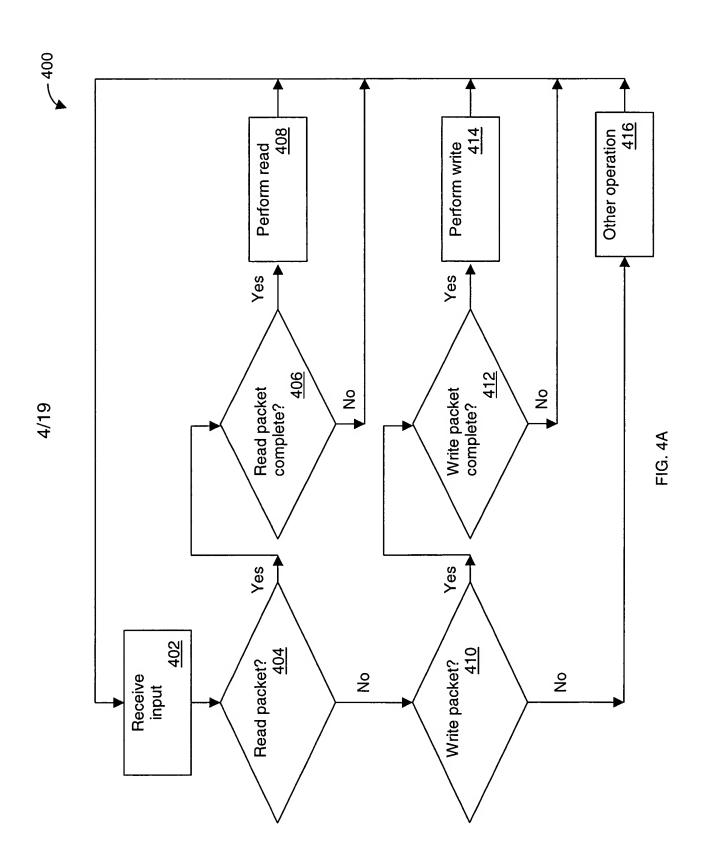
╁



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-<u>1</u>G. 3



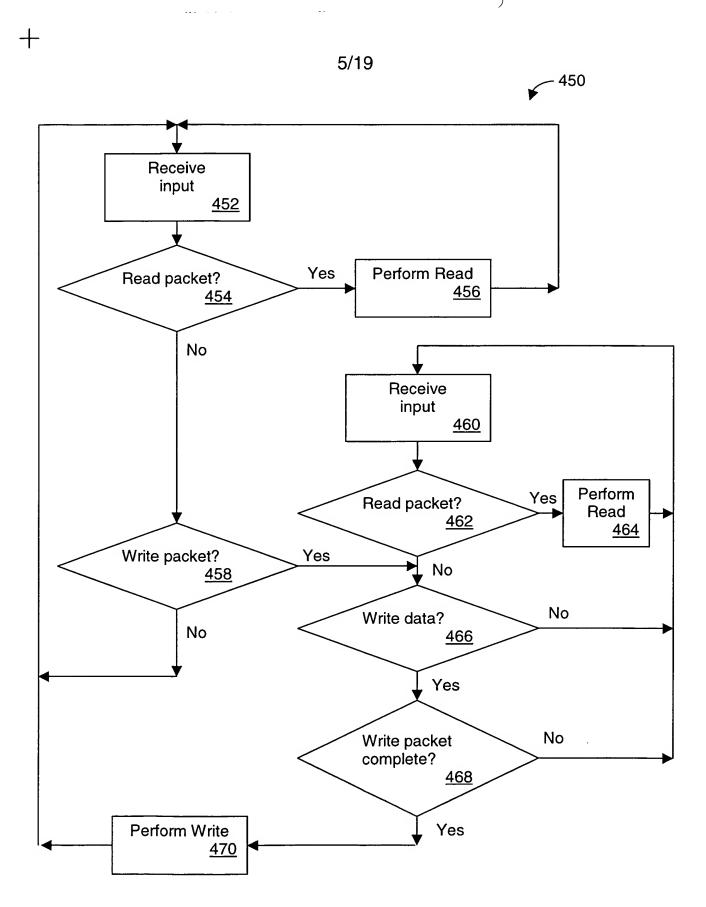
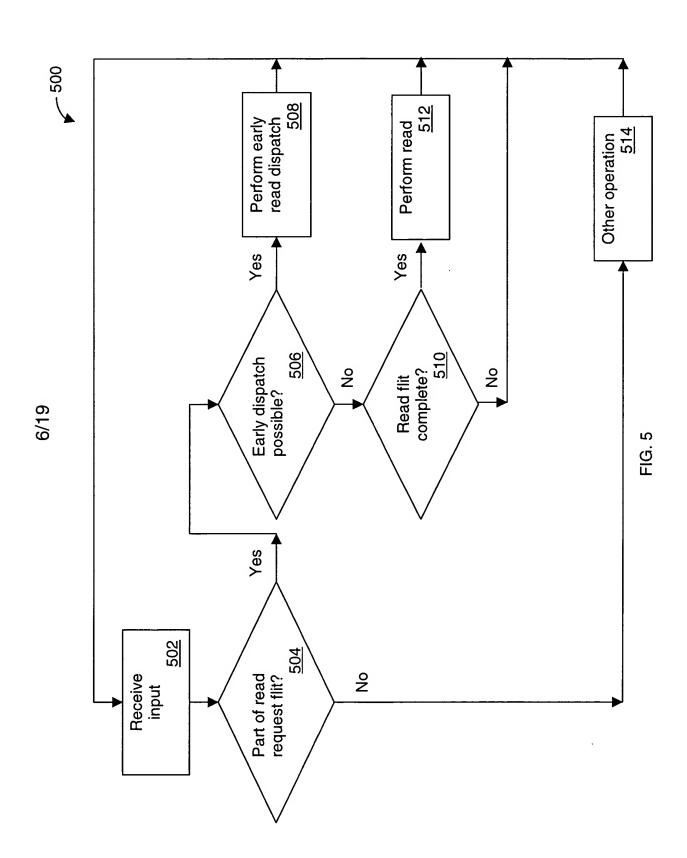


FIG. 4B



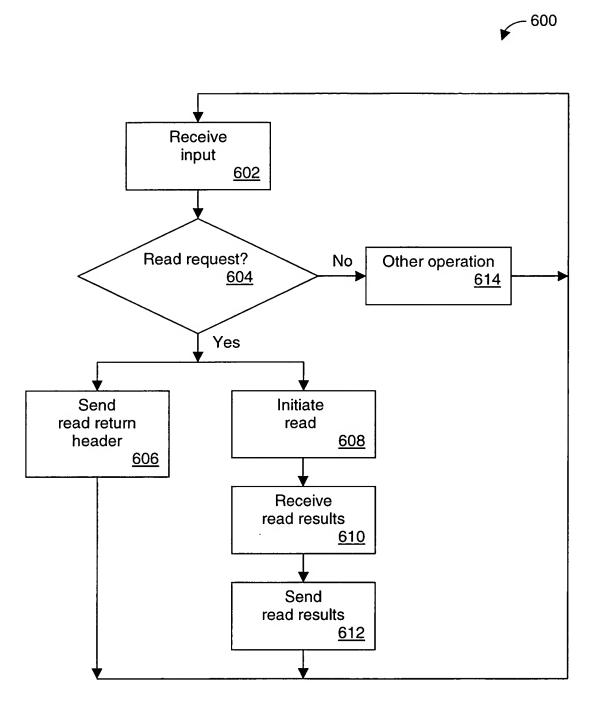


FIG. 6A



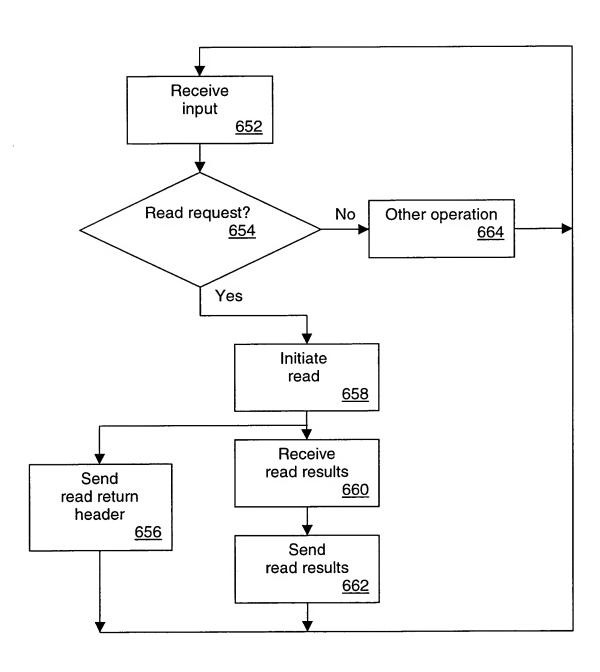
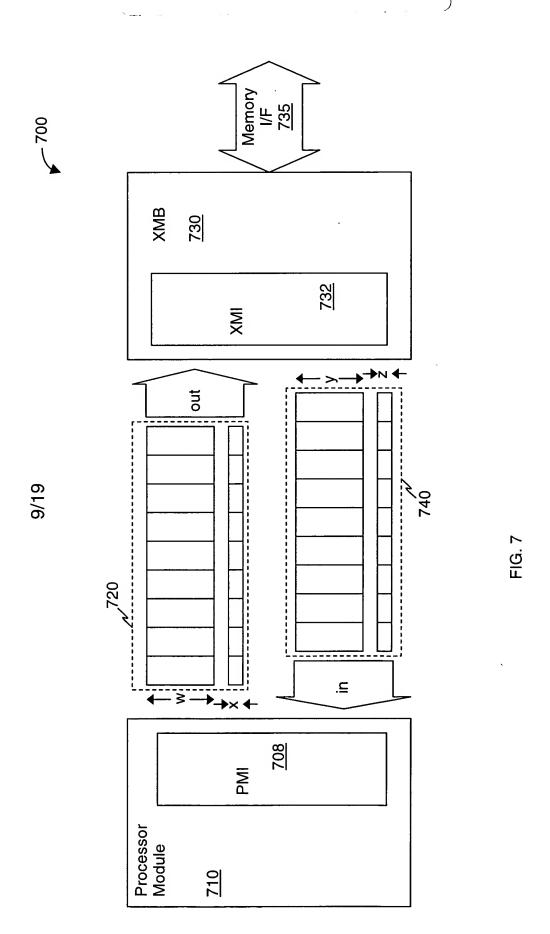


FIG. 6B



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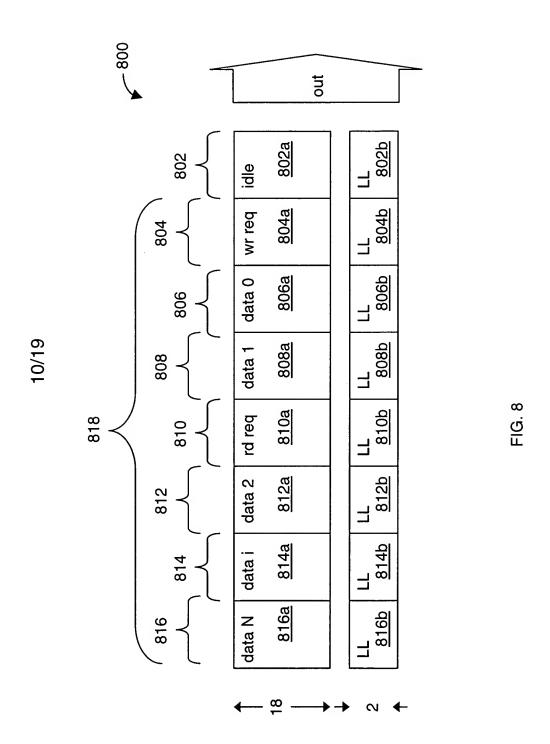
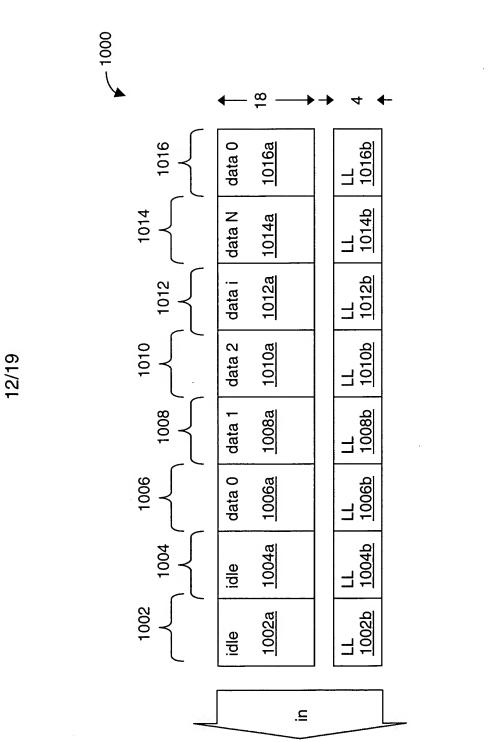
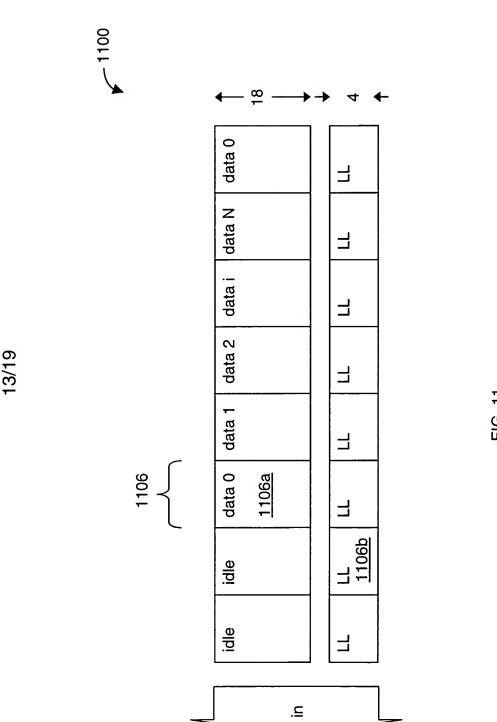


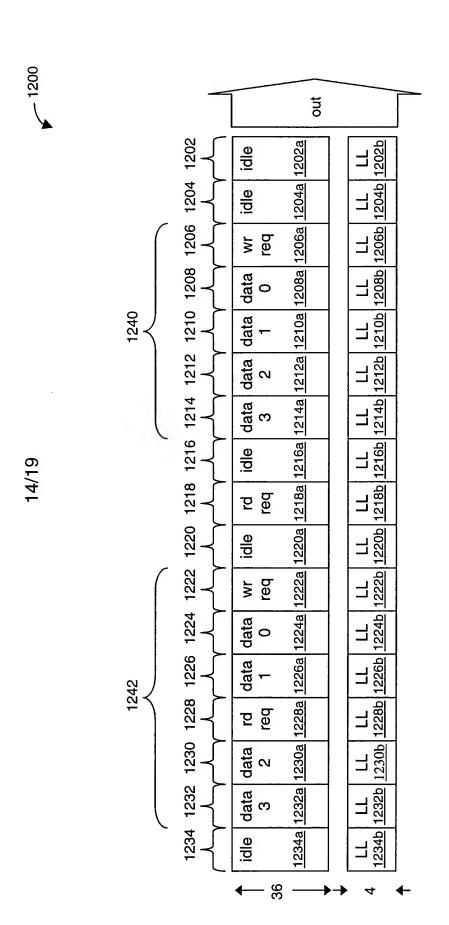
FIG. 9



:IG: 10

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G. 12

Transfer	BITS 17:0
	Lower Order Address Bits and Read/Write Command
	Higher Order Address Bits and Early Read Indicator
	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Stream ID,
	Size Bits, Cancel Command, Priority, etc.

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BITS 17:0	Lower Order Address Bits and Read/Write Command	Higher Order Address Bits and Early Read Indicator	oto offer dead from the offer of the open Transfer of the offer of the open of	_
↓Transfer	0	-	2	ဗ

FIG. 14

			otio otio	DIS, etc.
BITS 17:0	Lower Order Configuration Address Bits and Read/Write Command	Higher Order Configuration Address Bits and Early Read Indicator	Office Andreas Transcript Office from Address Transcript II Ober Bite Ato	initario Destination, Onset nom Address, Transaction ID, Onech Dits, Mash D
			Č	5
√Transfer	0	1	2	3

FIG. 15

- 1600

LL signals	Transfers 0:3
0	Info and Check Bits
1	Header, Tail, and Check Bits
2	Extended Mode Bits
3	Exterided Wode Bits

FIG. 16

- 1700

LL signals	Transfers 0:3
0	Type and Check Bits
1	Type and Offeck Bits
2	Info and Check Bits
3	Tho and oneck bits

FIG. 17

1800

LL signals	Transfers 0:3
0	Tag, Control, and Check Bits
1	rag, Control, and Check bits
2	Tag Info and Chack Pita
3	Tag, Info, and Check Bits

FIG. 18

1900

LL signals	Transfers 0:3
0	Tag and Check Bits
1	ray and oneck bits
2	Tag, Info, and Check Bits
3	

FIG. 19

___ 2000

LL signals	Transfers 0:3
0	Signal and Check Bits
1	Signal and Offect Dits
2	Signal, Info, Stop, and Check Bits
3	Signal, into, Stop, and Oneok bits